REMARKS

In the most recent office action, the Examiner rejected claims 1-13, 15-26 under 35 U.S.C. 103(a) as being unpatentable over Blumenau et al. (hereinafter "Blum", US Patent No. 6,421,711 B1) in view of Gunlock et al. (hereinafter "Gunlock", US Patent 6,952,734 B1). Claim 14 was considered unpatentable over Blum in view of Gunlock and further in view of Karpoff et al. (hereinafter "Karpoff", US Patent Publication 2002/0112113 A1).

Blum describes a storage controller with storage adapters associated with storage volumes and port adapters associated with a data network. (FIG. 1 and Col. 6, lines 65-67, Col. 7, lines 1-9) As can be seen from FIG. 1, the data network is between the hosts and the port adapters of the storage controller. (*Id.*) Essentially, the data network is constructed from switches (i.e., the switching circuit) positioned *not between* but external to the storage adapters and port adapters that make up the storage controller. (Col. 8, lines 46-55) FIG. 38 expressly shows and confirms that the switches 511, 512 and 513 are external to the cached subsystem and the subsytems contained therein.

Unfortunately, Blum does not teach or suggest "a switching circuit in the storage server that connects a plurality of storage processors and associates a first storage processor from the plurality of storage processors with said plurality of host computers and further associates a second storage processor from the plurality of storage processors with said plurality of storage devices,

wherein said plurality of storage processors in the storage server receive a plurality of command packets" as recited in claim 1.

In particular, Blum in FIG. 37 illustrates the switching circuit connected to a cached storage subsystem but not to a plurality of storage processors. Consistent with FIG. 37, FIG. 1 shows "cache memory" connected between storage adapters and port adapters of the cached storage subsystem . Indeed, the switching circuit, which is located in data network 21 (see Col. 8, lines 46-55), is external and "out of band" with respect to the storage adapters and port adapters and therefore cannot cause the storage processors to associate with the storage devices. For example, the storage adapters in Blum are connected to the cache memory and the storage devices but not to the switching circuit. It follows, therefore, that Blum does not have a switching circuit that connects a first storage processor to host computers and connect a second storage processor to the plurality of storage devices; the storage adapters in Blum are simply not directly or indirectly connected to the switching circuits.

Further, Blum also does not teach or suggest "a microengine in each of the plurality of storage processors to process said plurality of command packets and plurality of data packets using microcode and configure a routing path through said switching circuit to establish communication between the first storage processor and the second storage processor ,wherein the microcode executing on the microengines from one or more of the plurality of storage processors is responsive to at least one command packet of said plurality of command packets" as recited in claim 1.

Applicants have reviewed Blum and have not found where Blum teaches or suggests these further elements of claim 1. For example, Blum describes that any host may have access to any logical volume through one or more different paths but makes no mention of using the storage processors to calculate or determine such a path or route; Blum also mentions that a port may create a list of accessible LUNs in response to a "Report LUN" command. (Col. 9, lines 20-55) However, these descriptions do not teach or suggest "a microengine in each of the plurality of storage processors to process said plurality of command packets and plurality of data packets using microcode and configure a routing path through said switching circuit to establish communication between the first storage processor and the second storage processor" as recited in claim 1.

Blum also indicates that the logical storage volumes should have at least two independent paths to any logical volume but does not teach or suggest "configure a routing path through said switching circuit to establish communication between the first storage processor and the second storage processor" as recited in claim 1. (Col. 11, lines 56-65). Simply mentioning that it is preferable to have two or more routes or paths as stated in Blum is not sufficient to teach or suggest aspects of claim 1 as amended and filed. *In re Zurko,* 258 F. 3d 1379, 59 USPQ2d 1693 (Fed. Cir. 2001), *On remand from Dickinson v. Zurko,* 527 U.S. 150, 50 USPQ2d 1930 (1999) ("Feature missing from references; improper to rely on basic knowledge and common sense.")

Further, Blum indicates the need to restrict the set of volumes that can be seen by any one host. (Col. 12, lines 12-30). Indeed, Blum seems to have solved this problem by restricting

accessibility to sets of volumes to certain named groups.(*Id.*) Once again, this does teach or suggest, "a microengine in each of the plurality of storage processors to process said plurality of command packets and plurality of data packets using microcode and configure a routing path through said switching circuit to establish communication between the first storage processor and the second storage processor" as recited in claim 1. Unfortunately, there is nothing to indicate that the any storage processors are executing microcode on microengines and/or configuring a routing path therebetween.

Blum apparently also describes creating a stable ID, providing a path through the data network from a host controller to each port adapter and including a volume group name for the host controller in a volume access table in each port. (Col 13, lines 45-57) For example, providing a path from the host controller to each port adapter does not describe where the route came from or how it was calculated; this essentially remains a mystery with respect to Blum. Unfortunately, this does not teach, suggest or disclose, "a microengine in each of the plurality of storage processors to process said plurality of command packets and plurality of data packets using microcode and configure a routing path through said switching circuit to establish communication between the first storage processor and the second storage processor" as recited in claim 1.

As the Examiner has also noted, Blum also does not teach or suggest, "routing a data packet of said plurality of data packets over said path, prior to completely receiving said data packet, between said first storage processor and said second storage processor via said switching circuit". It

would also follow that Blum does not teach or suggest to "embed routing instructions for the routing path directly in each data packet of said plurality of data packets over said path using one or more microcode instructions in the microcode thereby allowing initial routing operations for a data packet between said first storage processor and said second storage processor through said switching circuit to take place prior to completely receiving said data packet in the entirety" as recited in claim 1.

The Examiner therefore indicated in the Office Action that Gunlock has a driver that uses "network information to determine header information and routing for the one or more fiber channel network frames or packets according to commands. The driver must determine an appropriate destination and routing for each frame required to implement a command, and transmit those frames over a port appropriate for that routing (column 1, lines 30-34, 61-64, column 2, lines 35-41,49-62, column 6, lines 56-62, column 7, lines 15-24)." According to the Examiner, Gunlock uses a driver to determine a route for each packet thus taking more time and processing. Gunlock therefore does not describe, teach or suggest embedding routing instructions directly in the packet as recited in claim 1 as amended.

For at least the above reasons, independent claim 1 as amended is allowable over Blum alone or in combination with Gunlock and/or Karpoff. Independent claim 19 and independent claim 24 are at least allowable for the same or similar reasons as claim 1. Dependent claims 2-18, 20-23 and 25-26, while each independently allowable, are also allowable by virtue of their dependence directly or indirectly on independent claims 1, 19 and 24 respectively.

Applicant respectfully submits that no new matter has been added by these claim amendments. Support for the amendments to the claims submitted herein can at least be found in paragraphs [86] through [143]. For example, the aforementioned paragraphs [86] through [143] further describe embedding routing instructions directly in the packet to improve performance and the use of microcode and microengines to facilitate this process.

Applicants have made a diligent effort to place the aforementioned claims in condition for allowance and respectively request allowance of the pending claims. Of course, should there remain unresolved issues or the Examiner believes a discussion appropriate, it is respectfully requested that the Examiner telephone Leland Wiesner, Applicants' Attorney at (650) 853-1113 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above remarks, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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